REMARKS

Claims 8-9, 12-15, 17, 19-21 and 30-32 are pending in the application. No claims have been amended. No claims have been added. No claims have been cancelled.

Rejections Under 35 U.S.C. § 103(a)

Claims 8-9, 12-14, and 30-32 have been rejected under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 6,477,623 of Jeddeloh ("Jeddeloh") in view of U.S. Patent No. 5,802,605 of Alpert et al. ("Alpert"). Applicants respectfully disagree. Jeddeloh discloses a GART table for translating addresses from a reserved range of graphics addresses into addresses containing graphic data that is scattered throughout the system memory. As disclosed, the GART table in Jeddeloh translates destination addresses originating from a number of different interfaces and devices coupled to a switch. However, as the Examiner indicated, Jeddeloh does not describe the use of a conversion table to translate two separate addresses, one from a graphics controller and another from a bus controller, into two different addresses that have a different number of bits than the original input address. That is, Jeddeloh doesn't disclose that the results of the address being output from the conversion table is greater in the number of bits than the address that is input to the conversion table.

The Examiner states that Alpert does disclose the conversion of addresses that result in addresses having a greater number of bits being output than are being input. Therefore, the Examiner believes it would be obvious to combine the address translation of Alpert into Jeddeloh to arrive at the present invention as claimed.

Applicants respectfully submit that it would not be obvious for one skilled in the art to combine Jeddeloh with Alpert to arrive at the present invention as claimed. The present invention is directed towards translation of addresses from graphics controllers and bus controllers using the same conversion table for the same memory. The present invention as claimed is directed towards finding mapping techniques from memory

that allows the address mapping techniques to be used with standard I/O busses and their attached peripherals, as well as graphics devices.

Data transfers directly between peripherals and main memory occur often. However, because they are limited to a certain number of address bits they often cannot access all of memory. Conventionally, this problem was solved by transferring data to and from the memory space through the accessible memory space and using separate software to transfer the data from the accessible memory space to a memory space that cannot be accessed due to the limit in the address bits. This process is very slow and places an unreasonable burden on the main memory bus. Jeddeloh is silent with respect such a problem.

Furthermore, Alpert is directed towards address translation performed in a processor. Therefore, the source of addresses is not from both a graphics controller and a bus controller, as set forth in the present invention as claimed. Therefore, Alpert is not directed to solving the same problem as solved by the present invention as claimed. Therefore, applicants respectfully submit one skilled in the art would not look to Jeddeloh and Alpert to arrive at the present invention as claimed.

Claims 15 and 17 have been rejected under 35 USC §103(a) as being unpatentable over Jeddeloh in view of Alpert and U.S. Patent No. 5,574,877 of Dixit ("Dixit"). As discussed above, the present invention as claimed sets forth converting addresses for a graphics controller and a bus controller using the same conversion table to generate addresses with a larger number of bits than the original input addresses. Neither Jeddeloh nor Dixit disclose this feature. Therefore, applicants respectfully submit that claims 15 and 17 are patentable over Jeddeloh in view of Dixit.

Claims 19-21 have been rejected under 35 USC §103(a) as being unpatentable over Jeddeloh in view of Dixit. Applicants respectfully submit, for the same reasons discussed above, that claims 19-21 are patentable over Jeddeloh in view of Dixit.

Accordingly, Applicants respectfully submit that the rejections under 35 U.S.C. § 103(a) have been overcome by the remarks, and withdrawal of these rejections is respectfully requested. Applicants submit that Claims 8-9, 12-15, 17, 19-21 and 30-32 are now in condition for allowance, and such action is earnestly solicited. Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 5, 2003.

Debra L. Riggio 8/5/2003
Date